Automotive CIS/CCM PMIC for Ultra Compact Camera and High Image Quality System

DESCRIPTION

The VE6200Q is an integrated PMIC with three step down converters and one high PSRR low-dropout (LDO) regulator for automotive camera applications. The high-voltage step down converter is operated with input voltage range up to 18.5V for Power Over Coax (POC) connection. Two low-voltage step down converters provide constant output voltage. All step down converters operate in a forced fixed-frequency PWM mode. The LDO output voltage is easily set via an external resistor. The VE6200Q provides 10 power sequences by a resistor for flexibility. The VE6200 is available in a QFN3X3-16 3x3 package with dimple lead type wettable flanks.

	PIN11	UVLO
VE6200QC-SEQL	SEQOUT	3.8V
VE6200QC-SEQH	SEQOUT	4.4V
VE6200QC-PGL	PG	3.8V
VE6200QC-PGH	PG	4.4V

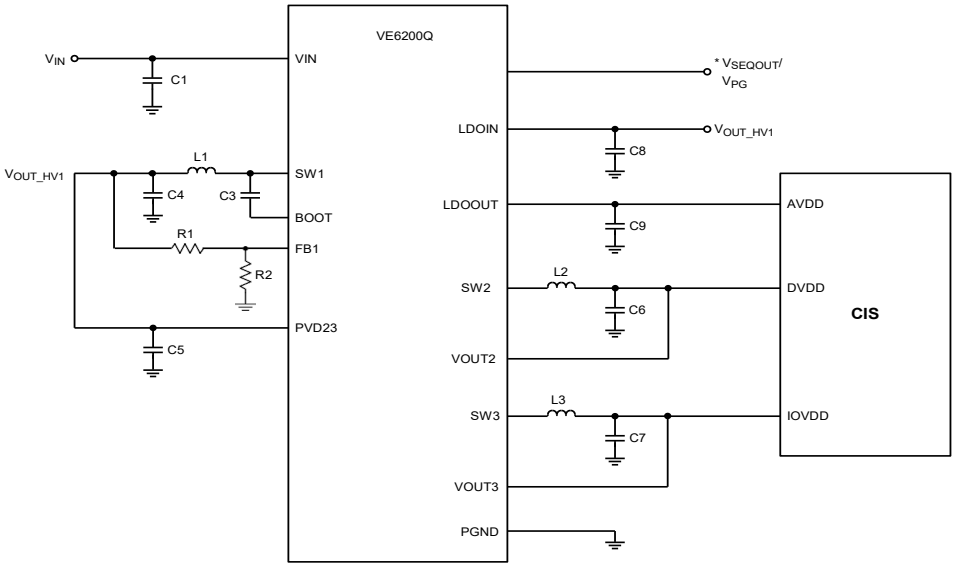
FEATURES

- AEC-Q100 Grade 1
- FMEA Compliant Pin Placement and Protection Mechanisms
- Three Step-Down Converters (HVBuck1, LVBuck2 and LVBuck3)
- Peak Current Mode PWM Operation
- Fixed Switching Frequency at 2.1MHz
- EMI Reduction with Spread Spectrum and Phase Shift
- Low Dropout Regulator (LDO)
- Input Voltage from 2.7V to 5V and 300mA Output Current
- 10 Adjustable Output Voltage Settings via RSET Pin
- High PSRR: 60dB at 100kHz, 40dB at 1MHz
- Small Form Factor QFN3X3-16 3x3 （Wettable Flanks Package）

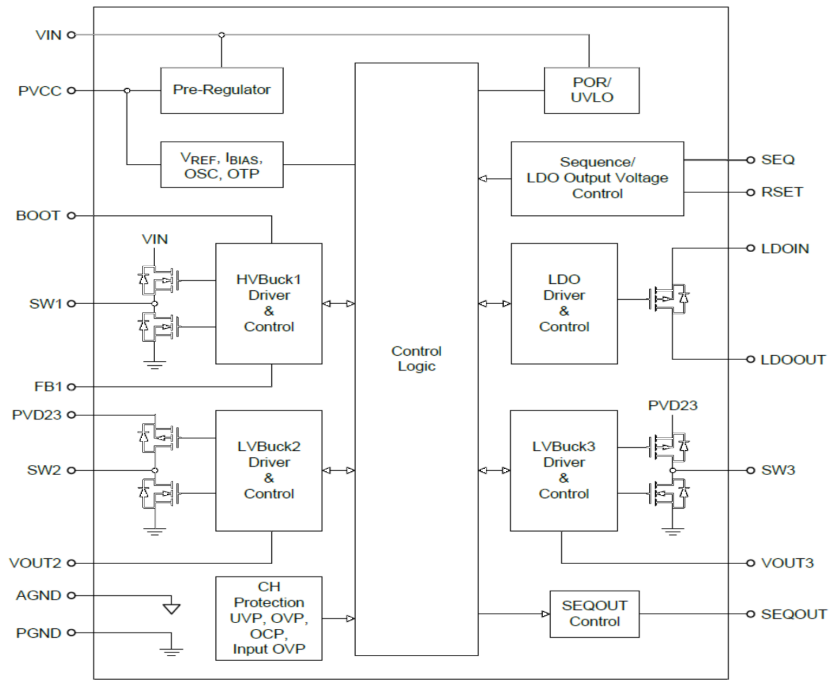
APPLICATIONS

- Automotive and Industrial Applications
- Battery-Powered Equipment

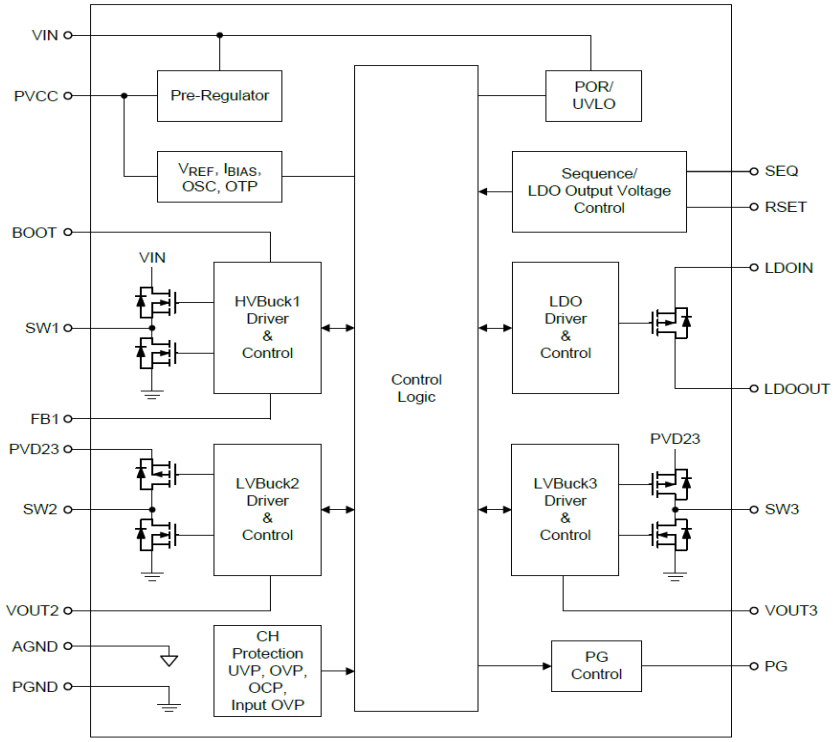
TYPICAL APPLICATION



BLOCK DIAGRAM



VE6200QC-SEQ

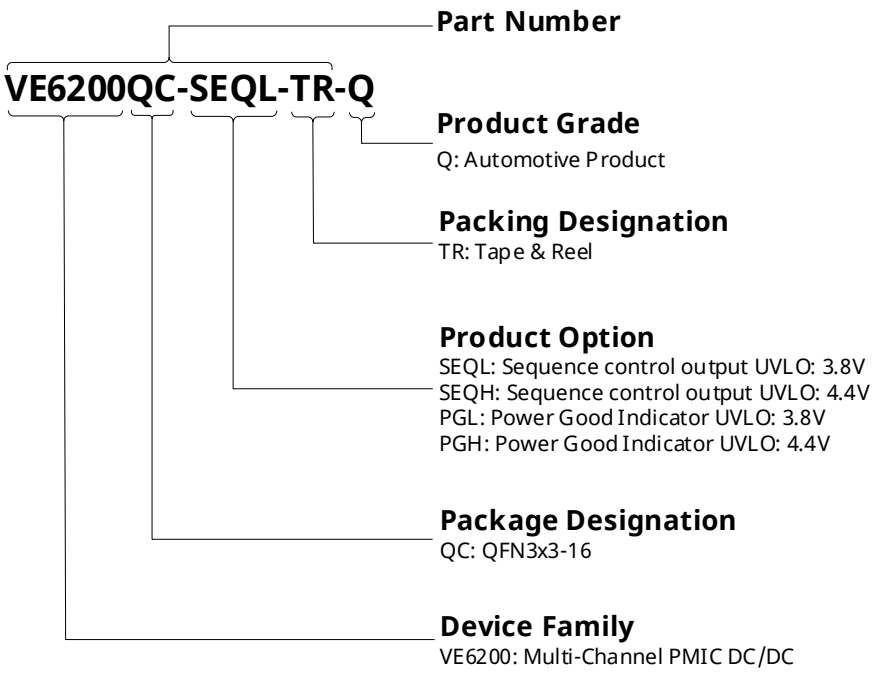


VE6200QC-PG

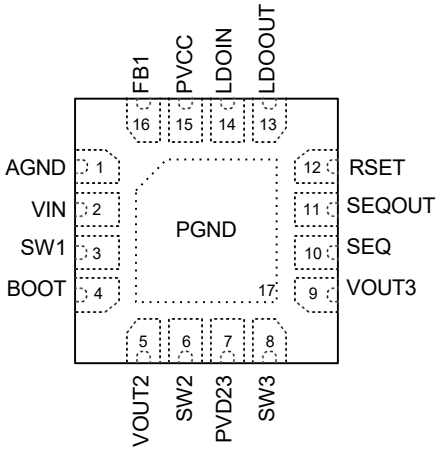
ORDERING INFORMATION

Ordering Information	Mark	Option	Class (1)	Temperature Range	Package	Pack	Quantity
VE6200QC-SEQL-TR	6200	SEQL	I	-40 to +125°C	QFN3x3-16	TR	5000
VE6200QC-SEQH-TR	6200	SEQH	I	-40 to +125°C	QFN3x3-16	TR	5000
VE6200QC-PGL-TR	6200	PGL	I	-40 to +125°C	QFN3x3-16	TR	5000
VE6200QC-PGH-TR	6200	PGH	I	-40 to +125°C	QFN3x3-16	TR	5000
VE6200QC-SEQL-TR-Q	6200	SEQL	Q	-40 to +125°C	QFN3x3-16	TR	5000
VE6200QC-SEQH-TR-Q	6200	SEQH	Q	-40 to +125°C	QFN3x3-16	TR	5000
VE6200QC-PGL-TR-Q	6200	PGL	Q	-40 to +125°C	QFN3x3-16	TR	5000
VE6200QC-PGH-TR-Q	6200	PGH	Q	-40 to +125°C	QFN3x3-16	TR	5000

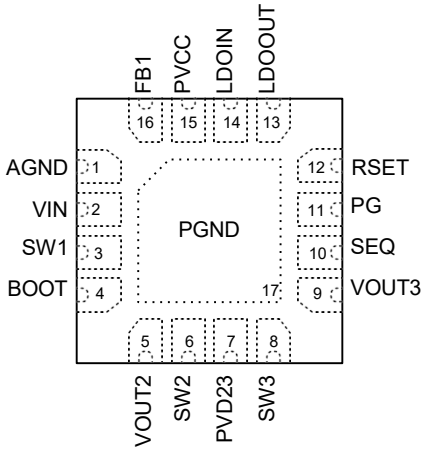
Note 1: The Class definition, Q=Automotive, I=Industrial.



PIN CONFIGURATIONS



QFN3X3-16-A



QFN3X3-16-B

PIN DESCRIPTION

Name	QFN3X3-16	Description
AGND	1	Analog ground.
VIN	2	Supply voltage input of HVBuck1. Connect a 4.7μF or larger decouple ceramic capacitor between this pin and ground.
SW1	3	HVBuck1 switch node.
BOOT	4	Bootstrap capacitor connection pin for HVBuck1. Connect a 0.1μF ceramic capacitor between this pin and SW1.
VOUT2	5	Output voltage feedback input of LVBuck2. Directly connect the output capacitor node to this pin for better regulation.
SW2	6	LVBuck2 switch node.
PVD23	7	Supply voltage input of LVBuck2 and LVBuck3. Connect a 4.7μF or larger decouple ceramic capacitor between this pin and ground.
SW3	8	LVBuck3 switch node.
VOUT3	9	Output voltage feedback input of LVBuck3. Directly connect the output capacitor node to this pin for better regulation.
SEQ	10	Power sequence selection.
SEQOUT (VE6200QC-SEQ)	11	Sequence control output with open drain structure for external power IC.
PG (VE6200QC-PG)		Power status indication pin with open drain structure for HVBuck1, LVBuck2, LVBuck3 and LDO. PG at high state indicates all outputs work well.
RSET	12	LDO output voltage selection.
LDOOUT	13	LDO output. Connect a 2.2μF ceramic decouple capacitor between this pin and ground.

Name	QFN3X3-16	Description
LDOIN	14	Supply voltage input of LDO. Connect a 2.2μF or larger decouple ceramic capacitor between this pin and ground.
PVCC	15	Internal analog power output. Connect a 1μF ceramic decouple capacitor between this pin and ground. Note additional external loading on this pin is forbidden.
FB1	16	Output voltage feedback input of HVBuck1.
PGND	17	IC thermal pad and power ground. It must connect to main ground plane for proper operation.

ABSOLUTE MAXIMUM RATINGS

Parameter	Minimum	Maximum	Unit
VIN	-0.3	+24	V
SW1	-0.3	+24	V
BOOT	-0.3	+28	V
BOOT to SW1	-0.3	+5	V
VOUT2, PVD23, VOUT3, SEQ, SEQOUT, PG, RSET, LDOOUT, LDOIN, PVCC, FB1	-0.3	+6.5	V
SW2, SW3	-0.3	+6.5	V

ESD RATINGS

Parameter	Value	Unit
Human Body Model (HBM), per AEC-Q100-002	3	kV
Charge Deice Model (CDM), per AEC-Q100-011	1	kV
Latch-Up, per AEC-Q100-004	100	mA

THERMAL INFORMATION

Thermal Resistance	θ_{JA}(°C/W)	θ_{JC}(°C/W)
QFN3X3-16	50	10

RECOMMENDED OPERATINIG CONDITIONS

Parameter	Minimum	Maximum	Unit
VIN	4	18.5	V
VPVD23, VLDOIN	2.7	5	V
Ambient Temperature	-40	+125	°C
Junction Temperature	-40	+150	°C

ECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 6V, V_{OUT_HV1}=3.6V, V_{OUT_LV2}=1.1V, V_{OUT_LV3}=1.8V, V_{OUT_LDO}=3.3V, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
System						
Under-Voltage Lockout Threshold	$UVLO_H$	V_{IN} rising	3.6	3.8	4	V
	$UVLO_L$	V_{IN} falling	3.15	3.3	3.45	V
Input Over-Voltage Protection	V_{IN_OV}		18.6	20	21.5	V
CH1 HVBuck1						
Input Voltage Range	V_{IN}		4	--	18.5	V
Output Voltage Range	V_{OUT_HV1}	Buck mode operation. Switching frequency, minimum on time and minimum off time need to be considered.	2.7	--	5	V
Output Feedback Voltage Accuracy	V_{FB1}		0.788	0.8	0.812	V
Switching Frequency	F_{SW_HV1}		1.89	2.1	2.31	MHz
Spread-Spectrum Range	SS_{HV1}		--	6	--	%
Switching Minimum On Time	$T_{ON\_MIN\_HV1}$		--	--	55	ns
Switching Minimum Off Time	$T_{OFF\_MIN\_HV1}$		--	--	50	ns
High-Side MOSFET On Resistance	$R_{ON\_HS\_HV1}$	From VIN pin to SW1 pin	115	210	340	mΩ
Low-Side MOSFET On Resistance	$R_{ON\_LS\_HV1}$	From SW1 pin to PGND pin	40	110	200	mΩ
Inductor Peak Current Limit	$I_{CL\_PK\_HV1}$		2.4	3	3.6	A
Inductor Valley Current Limit	$I_{CL\_VL\_HV1}$		--	2.7	--	A
Negative Inductor Peak Current Limit	$I_{CL\_NPK\_HV1}$			0.5		A
Output Discharge Resistor	R_{DIS_HV1}			270		Ω
Output Under-Voltage Falling Threshold	UVP_F_{HV1}		40	50	60	%
Output Feedback Over-Voltage Rising Threshold	OVP_R_{HV1}		--	110	--	%
CH2 LVBuck2 (V_{IN_PVD23} = 3.6V)						
Input Voltage Range	V_{IN_PVD23}		2.7	--	5	V
Output Voltage	V_{OUT_LV2}		--	1.1	--	V
Output Voltage Accuracy	$V_{OUT\_ACC\_LV2}$		−1.5	--	1.5	%
Switching Frequency	F_{SW_LV2}		1.89	2.1	2.31	MHz
Spread-Spectrum Range	SS_{LV2}		--	6	--	%

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Switching Minimum On Time	$T_{ON\_MIN\_LV2}$		--	--	44	ns
High-Side MOSFET On Resistance	$R_{ON\_HS\_LV2}$	From PVD23 pin to SW2 pin	110	150	215	mΩ
Low-Side MOSFET On Resistance	$R_{ON\_LS\_LV2}$	From SW2 pin to PGND pin	60	90	145	mΩ
Inductor Peak Current Limit	$I_{CL\_PK\_LV2}$		1.8	2.2	2.6	A
Inductor Valley Current Limit	$I_{CL\_VL\_LV2}$		--	1.8	--	A
Negative Inductor Peak Current Limit	$I_{CL\_NPK\_LV2}$			0.964		A
Output Discharge Resistor	R_{DIS_LV2}			9		Ω
Output Under-Voltage Falling Threshold	$UVP_{\_F\_LV2}$		40	50	60	%
Output Over-Voltage Rising Threshold	$OVP_{\_R\_LV2}$		--	120	--	%
Output Over-Voltage Falling Threshold	$OVP_{\_F\_LV2}$		--	110	--	%
Input Over-Voltage Rising Threshold	$OVP_{\_IN\_R\_LV2}$		5.35	5.8	6.25	V
Input Over-Voltage Hysteresis	$OVP_{\_IN\_HYS\_LV2}$	V_{IN_PVD23} falling	--	580	--	mV
CH3 LVBuck3 (V_{IN_PVD23} = 3.6V)						
Input Voltage Range	V_{IN_PVD23}		2.7	--	5	V
Output Voltage	V_{OUT_LV3}		--	1.8	--	V
Output Voltage Accuracy	$V_{OUT\_ACC\_LV3}$		-1.5	--	1.5	%
Switching Frequency	F_{SW_LV3}		1.89	2.1	2.31	MHz
Spread-Spectrum Range	$SS_{\_LV3}$		--	6	--	%
Switching Minimum On Time	$T_{ON\_MIN\_LV3}$		--	--	44	ns
High-Side MOSFET On Resistance	$R_{ON\_HS\_LV3}$	From PVD23 pin to SW3 pin	240	310	440	mΩ
Low-Side MOSFET On Resistance	$R_{ON\_LS\_LV3}$	From SW3 pin to PGND pin	170	230	360	mΩ
Inductor Peak Current Limit	$I_{CL\_PK\_LV3}$		0.96	1.3	1.6	A
Inductor Valley Current Limit	$I_{CL\_VL\_LV3}$		--	1.08	--	A
Negative Inductor Peak Current Limit	$I_{CL\_NPK\_LV3}$			0.6		A
Output Discharge Resistor	R_{DIS_LV3}			10		Ω
Output Under-Voltage Falling Threshold	$UVP_{\_F\_LV3}$		40	50	60	%
Output Over-Voltage Rising Threshold	$OVP_{\_R\_LV3}$		--	120	--	%
Output Over-Voltage Falling Threshold	$OVP_{\_F\_LV3}$		--	110	--	%
Input Over-Voltage Rising	$OVP_{\_IN\_R\_LV3}$		5.35	5.8	6.25	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Threshold						
Input Over-Voltage Hysteresis	$OVP_{IN\_HYS\_LV3}$	V_{IN_PVD23} falling	--	580	--	mV
CH4 LDO (VIN_LDO = 3.6V)						
Input Voltage Range	V_{IN_LDO}		2.7	--	5	V
Output Voltage Range	V_{OUT_LDO}	V_{OUT_LDO} setting via RSET	1.8	--	3.5	V
Output Voltage Accuracy	$V_{OUT\_ACC\_LDO}$	V_{IN_LDO} - V_{OUT_LDO} > 0.3V, I_{OUT_LDO} = 0mA to 300mA	-1.5	--	1.5	%
Maximum Output Current	$I_{OUT\_MAX\_LDO}$		300	--	--	mA
Dropout Voltage	$V_{DROP\_300\_LDO}$	I_{OUT_LDO} = 300mA (Note 5)	--	--	300	mV
	$V_{DROP\_150\_LDO}$	I_{OUT_LDO}=150mA (Note 5)	--	--	150	
Output Current Limit	I_{CL_LDO}	(Note 6)	345	450	555	mA
Output Discharge Resistor	R_{DIS_LDO}		48	76	104	Ω
Output Under-Voltage Falling Threshold	UVP_{F_LDO}		30	40	50	%
Output Over-Voltage Rising Threshold	OVP_{R_LDO}		--	125	--	%
Output Over-Voltage Falling Threshold	OVP_{F_LDO}		--	110	--	%
Input Over-Voltage Rising Threshold	$OVP_{IN\_R\_LDO}$		5.35	5.8	6.25	V
Input Over-Voltage Hysteresis	$OVP_{IN\_HYS\_LDO}$	V_{IN_LDO} falling	--	500	--	mV
PVCC (Note 7)						
Internal Regulator Output Voltage	V_{OUT_PVCC}		4.33	4.58	4.83	V
Over-Current Limit	I_{CL_PVCC}		150	--	300	mA
SEQOUT (VE6200QC-SEQ)						
Output Low Voltage		Current into SEQOUT pin equal to 2mA	--	--	230	mV
Input Leakage Current	I_{LEAK_SEQOUT}	1.8V applied on SEQOUT pin	--	--	1	μA
Power Good (VE6200QC-PG)						
Pull Down Voltage	$V_{OUT\_L\_PG}$	Current into PG pin equal to 5mA	--	--	200	mV
Input Leakage Current	I_{LEAK_PG}	1.8V applied on PG pin	--	--	1	μA
Timing						
Soft-Start Time	T_{SS_HV1}	Time from V_{OUT_HV1} 0% rise to 90% of target value, no load	500	1000	1500	μs

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
	T_{SS_LV2}	Time from V_{OUT_LV2} 0% rise to 90% of target value, no load	500	1000	1500	
	T_{SS_LV3}	Time from V_{OUT_LV3} 0% rise to 90% of target value, no load	500	1000	1500	
	T_{SS_LDO}	Time from the previous turn on channel's output voltage reaching 90% of target value to V_{OUT_LDO} rise to 90% of target value.	200	700	1100	
PG Delay Time	T_{DLY_PG}	(VE6200QC-PG)	9	10	11	ms

SYSTEM CHARACTERISTICS

The following specifications are guaranteed by design and are not performed in production testing.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
System						
Over-Temperature Protection	OTP		--	160	--	°C
Over-Temperature Protection Hysteresis	OTP_H		--	20	--	°C
CH1 HVBuck1						
Maximum Output Current	$I_{OUT\_MAX\_HV1}$		2	--	--	A
Load Regulation	$V_{LOAD\_REG\_HV1}$	I_{OUT_HV1} = 0A to 2A	--	--	0.1	%/A
Line Regulation	$V_{LINE\_REG\_HV1}$	V_{IN} = 5V to 18.5V, I_{OUT_HV1} = 2A	--	--	1	%
Load Transient	$V_{LOAD\_TRAIN\_HV1}$	I_{OUT_HV1} = 10mA to 500mA to 10mA, 1μs	–150	--	150	mV
Line Transient	$V_{LINE\_TRAIN\_HV1}$	V_{IN} = 5V to 18.5V to 5V, 100μs, I_{OUT_HV1} = 10mA/500mA	–50	--	50	mV
Output Ripple	V_{RIPPLE_HV1}	Peak to peak in one switching cycle	--	--	20	mVpp
CH2 LVBuck2 (V_{IN_PVD23} = 3.6V)						
Maximum Output Current	$I_{OUT\_MAX\_LV2}$		1.5	--	--	A
Load Regulation	$V_{LOAD\_REG\_LV2}$	I_{OUT_LV2} = 0A to 1.5A	--	--	0.1	%/A
Line Regulation	$V_{LINE\_REG\_LV2}$	V_{IN_PVD23} = 2.7V to 5V, I_{OUT_LV2} = 1.5A	--	--	1	%
Load Transient	$V_{LOAD\_TRAIN\_LV2}$	I_{OUT_LV2} = 10mA to 500mA to 10mA, 1μs	–50	--	50	mV
Line Transient	$V_{LINE\_TRAIN\_LV2}$	V_{IN_PVD23} = 3V to 5V to 3V, 50μs, I_{OUT_LV2} = 10mA/1A	–50	--	50	mV
Output Ripple	V_{RIPPLE_LV2}	Peak to peak in one switching cycle	--	--	10	mVpp

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CH3 LVBuck3 (V_{IN_PVD23} = 3.6V)						
Maximum Output Current	$I_{OUT\_MAX\_LV3}$		700	--	--	mA
Load Regulation	$V_{LOAD\_REG\_LV3}$	I_{OUT_LV3} = 0A to 750mA	--	--	0.1	%/A
Line Regulation	$V_{LINE\_REG\_LV3}$	V_{IN_PVD23} = 2.7V to 5V, I_{OUT_LV3} = 750mA	--	--	1	%
Load Transient	$V_{LOAD\_TRAIN\_LV3}$	I_{OUT_LV3} = 10mA to 300mA to 10mA, 1μs	–50	--	50	mV
Line Transient	$V_{LINE\_TRAIN\_LV3}$	V_{IN_PVD23} = 3V to 5V to 3V, 50μs, I_{OUT_LV3} = 10mA/300mA	–50	--	50	mV
Output Ripple	V_{RIPPLE_LV3}	Peak to peak in one switching cycle	--	--	10	mVpp
CH4 LDO (V_{IN_LDO} = 3.6V)						
Power Supply Rejection Ratio	$PSRR_{\_LDO}$	I_{OUT_LDO} = 100mA, f = 100kHz	--	60	--	dB
		I_{OUT_LDO} = 100mA, f = 1MHz	--	40	--	
Output Noise Voltage	$eN_{\_LDO}$	I_{OUT_LDO} = 100mA, f = 100Hz to 100kHz	--	60	--	μV
Load Transient	$V_{LOAD\_TRAIN\_LDO}$	I_{OUT_LDO} = 10mA to 200mA to 10mA, 1μs	–25	--	25	mV
Line Transient	$V_{LINE\_TRAIN\_LDO}$	All V_{OUT_LDO}, V_{IN_LDO} step 600mV, LDO not in dropout condition, 10μs, I_{OUT_LDO} = 1mA/300mA	–25	--	25	mV
Component Requirement (Note 4)						
Effective Input Capacitance	C_{IN_HV1}		1.5	4.7	10	μF
	C_{IN_PVD23}		1.5	4.7	10	
	C_{IN_LDO}		0.7	2.2	4	
Effective Output Capacitance	C_{OUT_HV1}		3.3	10	14	μF
	C_{OUT_LV2}		4.5	10	14	
	C_{OUT_LV3}		4.5	10	14	
	C_{OUT_LDO}		0.7	2.2	4	
Output Inductance	L_{HV1}		1	1.5	2	μH
	L_{LV2}		0.68	1	1.2	
	L_{LV3}		0.68	1	1.2	
Effective Boot Capacitance	C_{BOOT}		0.07	0.1	0.13	μF
Effective PVCC Capacitance	C_{PVCC}		0.3	1	1.4	μF

Note 1： Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2： θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{Jc} is measured at the exposed pad of the package.

Note 3.： Devices are ESD sensitive. Handling precaution is recommended.

Note 4： The device is not guaranteed to function outside its operating conditions.

Note 5： Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

Note 6： It only supports LDO loading smaller than 150mA (typ.) to power up successfully. The current limit changes back to 450mA after LDO rail enabled after 8ms.

Note 7： PVCC is the pre-regulator output voltage only for internal circuitry. External loading on PVCC pin is forbidden.

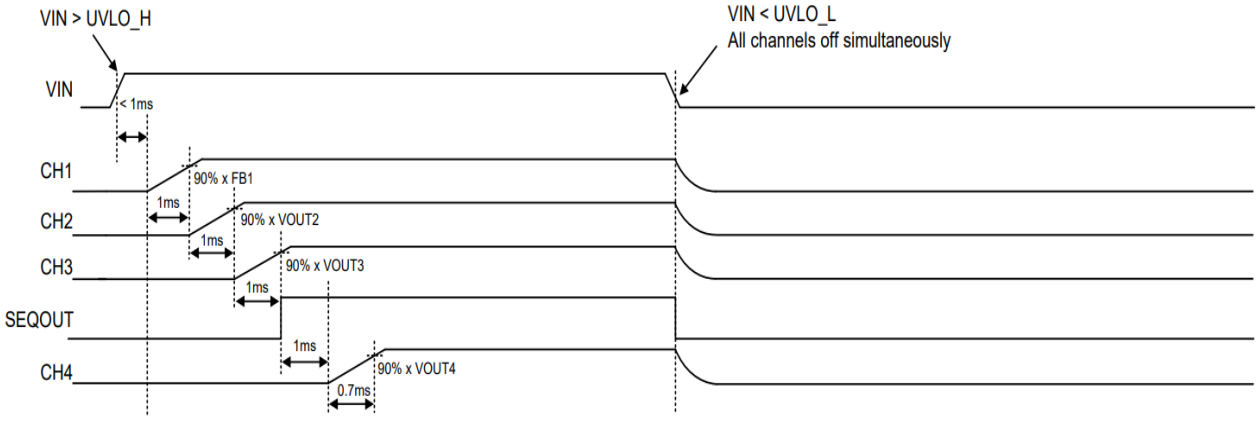
FUNCTION DESCRIPTION

Power Sequence Control

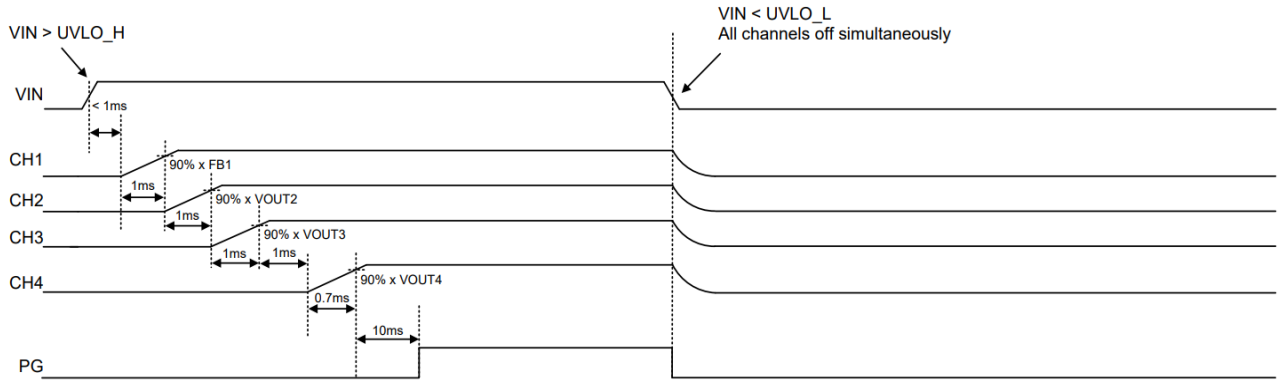
The VE6200QC-SEQ/VE6200QC-PG supports 10 power-on sequences for the step-down converters and LDO via the dedicated resistor on SEQ pin. SEQ pin is not allowable at floating state and resistance selected out of range is not guaranteed to correct power-on sequence. In addition, there is only simultaneous power-off for all outputs. To fix the resistor selection on SEQ pin before enabling the device. Any change during the power on procedure is not guarantee to the correct power-on sequence. Below table shows the power-on sequence with its corresponding resistance.

Table1 : Power-On Sequence Control

SEQ No.	Resistance on SEQ (Ω)			Sequence				
	Min	Typ	Max					
SEQ0	1.07M	1.1M	1.13M	CH1	CH4	CH3	CH2	SEQOUT
SEQ1	319	330k	341k	CH1	CH2	CH3	SEQOUT	CH4
SEQ2	164k	169k	174k	CH1	CH2	SEQOUT	CH3	CH4
SEQ3	81.6k	84.5k	87.4k	CH1	SEQOUT	CH2	CH4	CH3
SEQ4	45.4k	47k	48.6k	CH1	CH2, CH3, CH4, SEQOUT			
SEQ5	26.1k	27k	27.9k	CH1, CH2, CH3, CH4, SEQOUT				
SEQ6	14.5k	15k	15.5k	CH1	CH3	CH2	CH4	SEQOUT
SEQ7	7.78k	8.06k	8.34k	CH1	CH3	CH4	CH2	SEQOUT
SEQ8	Short to PVCC			CH1	SEQOUT	CH2	CH3	CH4
SEQ9	Short to PGND			CH1	CH2	CH3	CH4	SEQOUT



Example SEQ1 for VE6200QC-SEQ



Example SEQ1 for VE6200QC-PG

Output Voltage Setting

- **HVBuck1**

The output voltage set by external feedback resistors expressed in the following equation.

$$V_{OUT\_HV1}=\left(1+\frac{R_1}{R_2}\right)*V_{FB1}$$

Where the reference voltage V_{FB1} is 0.8V (typ.)

The placement of the resistive divider should be as close as possible to the FB1 pin. For better output voltage accuracy, the divider resistors with ±1% tolerance or better should be used. The resistance ranges from few kΩ to hundreds of kΩ is recommended.

- **LVBuck2 and LVBuck3**

The output voltage of LVBuck2 is fixed 1.1V. The output voltage of LVBuck3 is fixed 1.8V.

- **LDO**

The LDO output voltage is controlled by setting the dedicated resistor on RSET pin. RSET pin is not allowable at floating state and resistance selected out of range is not guaranteed to correct output voltage. Changing of the output voltage real time is not recommended. To fix the resistor selection on RSET pin before enabling the device.

Table 2 : LDO Output Voltage

REST No.	Resistance on REST (Ω)			Voltage(V)
	Min	Typ	Max	
REST0	1.07M	1.1M	1.13M	3.5
REST 1	319k	330k	341k	3.4
REST 2	164k	169k	174k	3.2
REST 3	81.6k	84.5k	87.4k	3.1
REST 4	45.4k	47k	48.6k	3.0
REST 5	26.1k	27k	27.9k	2.8
REST 6	14.5k	15k	15.5k	2.7
REST 7	7.78k	8.06k	8.34k	1.8
REST 8	Short to PVCC			2.9
REST 9	Short to PGND			3.3

Channel Protection Features

The VE6200QC-SEQ/VE6200QC-PG equips protections to prevent the device from damages causing by abnormal operations or fault conditions. (Over-load, Short-circuit, Soldering issue…etc.)

- **Under-Voltage Protection (UVP)**

▸ HVBuck1, LVBuck2, LVBuck3 and LDO

The device disables all channels and enters into latch off state if step-down converter or LDO output under voltage fault detected continuously over deglitch time and the device only can re-start with V_{IN} ON/OFF.

- **Over-Voltage Protection (OVP)**

▸ HVBuck1

When FB1 pin over-voltage fault detected, the high-side and low-side MOSFETs turn off immediately and auto-recover to switch until FB1 pin's voltage decrease to the reset level.

▸ LVBuck2, LVBuck3 and LDO

The device disables all channels when step-down converter or LDO output over-voltage fault detected continuously over deglitch time. When the fault released, the device auto-restarts all channels in sequence.

- **Over-Current Protection (OCP)**

▸ HVBuck1, LVBuck2 and LVBuck3

The step-down converter includes a cycle-by-cycle high-side MOSFET peak current-limit protection against the condition that the inductor current increasing abnormally, even over the inductor saturation current rating. If an over-current condition occurs, the controller will immediately turn off the high-side MOSFET and turn on the low-side MOSFET to prevent the inductor current exceeding the peak current limit level. After inductor current decreasing to below the valley current limit, the high-side MOSFET resume switching on. If over-current fault further detected continuously over than deglitch time, the device disables all channels and enters into latch off state and the device only can re-start with VIN ON/OFF.

▸ **LDO**

When the load reaches the current limit threshold, the current sent to the output will kept at current limit level. If over-current fault detected continuously over than the deglitch time, the device disables all channels and enters into latch off state and the device only can re-start with V_{IN} ON/ OFF.

- **Input Over-Voltage Protection (OVP)**

▸ LVBuck2, LVBuck3 and LDO

If the input voltage of step-down converters (LVBuck2, LVBuck3) or LDO reaches over-voltage protection level, the device disables all channels. After fault removed, it auto-restarts all channels in sequence.

Channel	Type	Threshold (Typ.)	Deglitch	Protection	Reset and Threshold (Typ.)
System	UVLO	$V_{IN} \le 3.3V$ (after IC Operation)	32μs	Disable all channels	$V_{IN} \ge 3.8V$
	OVP	$V_{IN} \ge 20V$	5ms	Disable all channels then latch-off protection	$V_{IN} \le 3.3V$, then $V_{IN} \ge 3.8V$
	OTP	$T_J \ge 160°C$	5μs	Disable all channels then latch-off protection	$T_J \le 140°C$ and $V_{IN} \le 3.3V$, then $V_{IN} \ge 3.8V$
CH1 HVBuck1	UVP	$V_{FB1} \le 0.8V \times 50\%$	5μs	Disable all channels then latch-off protection	$V_{IN} \le 3.3V$, then $V_{IN} \ge 3.8V$
	OVP	$V_{FB1} \ge 0.8V \times 110\%$	NA	High/Low-side MOSFETs off, low-side MOSFET conditionally ON to charge the BOOT capacitor for	$V_{FB1} < 0.8V \times 110\%$

Channel	Type	Threshold (Typ.)	Deglitch	Protection	Reset and Threshold (Typ.)
				driving high-side MOSFET.	
	OCP	I_{L1_peak} ≥ 3A	10ms	Cycle-by-cycle detection If keep 10ms, disable all channels then latch-off protection.	If latch-off protection, V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
CH2 LVBuck2	UVP	V_{OUT_LV2} ≤ 1.1V x 50%	5μs	Disable all channels then latch-off protection	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	OVP	V_{OUT_LV2} ≥ 1.1V x 120%	5ms	Disable all channels	V_{OUT2} ≤ 1.1V x 110% with deglitch 5ms
	OCP	I_{L2_peak} ≥ 2A	10ms	Cycle-by-cycle detection If keep 10ms, disable all channels then latch-off protection.	If latch-off protection, V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	Input OVP	V_{IN_PVD23} ≥ 5.8V	5μs	Disable all channels	V_{IN_PVD23} ≤ 5.22V with deglitch 5μs
CH3 LVBuck3	UVP	V_{OUT_LV3} ≤ 1.8V x 50%	5μs	Disable all channels then latch-off protection	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	OVP	V_{OUT_LV3} ≥ 1.8V x 120%	5ms	Disable all channels	V_{OUT3} ≤ 1.8V x 110% with deglitch 5ms
	OCP	I_{L3_peak} ≥ 1.2A	10ms	Cycle-by-cycle detection If keep 10ms, disable all channels then latch-off protection.	If latch-off protection, V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	Input OVP	V_{IN_PVD23} ≥ 5.8V	5μs	Disable all channels	V_{IN_PVD23} ≤ 5.22V with deglitch 5μs
CH4 LDO	UVP	V_{OUT_LDO} ≤V_{OUT_LDO} setting x 40%	5μs	Disable all channels then latch-off protection	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	OVP	V_{OUT_LDO} ≥ V_{OUT_LDO} x 125%	5ms	Disable all channels	V_{OUT_LDO} ≤ V_{OUT_LDO} x 110% with deglitch 5ms
	OCP	I_{OUT_LDO} ≥ 450mA	10ms	Disable all channels then latch-off protection	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	Input OVP	V_{IN_LDO} ≥ 5.8V	5μs	Disable all channels	V_{IN_LDO} ≤ 5.3V with deglitch 5μs

Input and Output Capacitor Selection

- **HVBuck1, LVBuck2 and LVBuck3**

It is recommended at least a 4.7μF input capacitor with a 10μF output capacitor for step-down converters. The ripple voltage is an important index for choosing output capacitor. This portion consists of two parts. One is the product of ripple current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. The output ripple can be calculated as below.

$$\Delta I_{OUT_{RIPPLE}} = \Delta V_{ESR} + \Delta V_{OUT} = \Delta V_{ESR} + \frac{\Delta I_L}{8F_{SW} \times C_{OUT}}$$

Where $\Delta V_{ESR} = I_{CRMS} \times R_{CESR}$

- **LDO**

Like any low dropout regulator, the external capacitor of the VE6200Q must be carefully selected for regulator stability and performance. Using a 2.2μF capacitor for the LDO's input and output is suitable.

Additional capacitor paralleled on the output may get better noise suppression but also lead to higher input inrush current when LDO outputs. It should be taken into consideration carefully.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to- ambient thermal resistance, θ_{JA}, is highly package dependent. For a QFN3X3-16 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four- layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below:

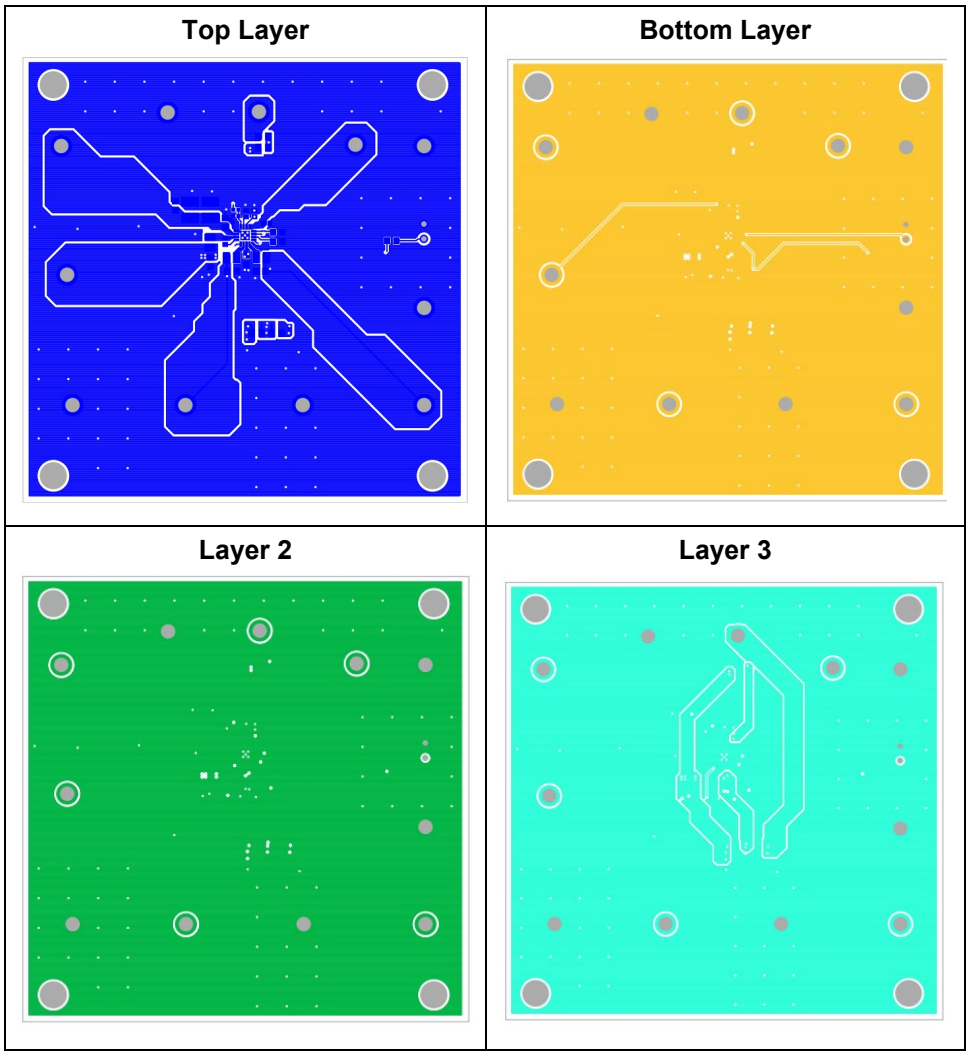
$P_{D(MAX)}$ = (150°C – 25°C) / (30°C/W) = 4.16W for a QFN3X3-16 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}.

PCB Layout Guidelines

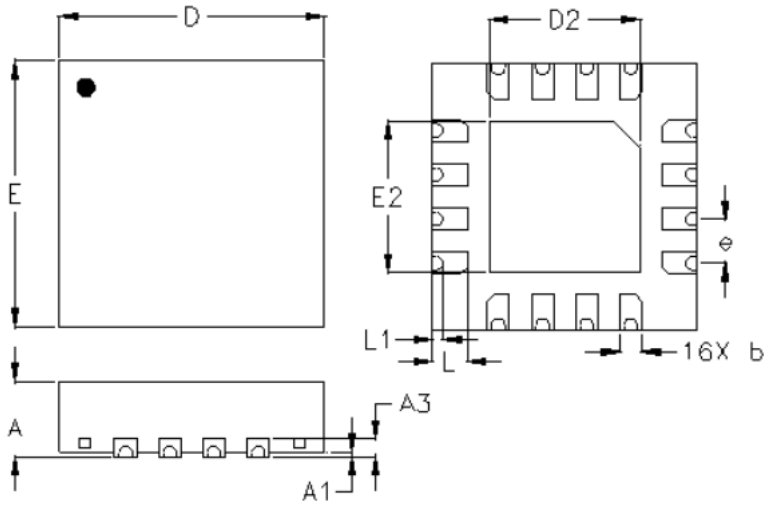
The PCB layout is an important step to maintain the high performance of the VE6200Q. Both the high current and the fast switching nodes demand full attention to the PCB layout to keep the robustness of the VE6200Q through the PCB layout. Improper layout might lead to the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the VE6200Q, the following PCB layout guidelines must be strictly followed.

1. The trace from switching node to inductor should be as short as possible to be minimized the switching loop for better EMI.
2. Place the input and output capacitors close to the input and output pins respectively for good filtering.
3. Keep the main power traces as wide and short as possible.
4. Connect the AGND and PGND to a strong ground plane for maximum thermal dissipation and noise protection.
5. Directly connect the step-down converter's output capacitor to the feedback network to avoid bouncing caused by parasitic resistance and inductance from the PCB trace.



PACKAGE INFORMATION

QFN3X3-16



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.65	1.750	0.065	0.069
E	2.950	3.050	0.116	0.120
E2	1.650	1.750	0.065	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018
L1	0.075	0.175	0.003	0.007

REVISION HISTORY

Revision	Data	Description
1.0	2024-10-18	Initial Release